

REMARKS

Claims 1 through 7, 9 through 16 and 18 through 20 are currently pending in the application.

This amendment is in response to the Office Action of May 7, 2003.

In the "Detailed Action" item 2 of the Official Action of May 7, 2003, the Official Action states

that the instant application does not explicitly describe "the north bridge" in any specific definition or description, thus it is considered for art rejection purpose, the claimed "north bridge chip" is interpreted as a "logic chip" that has the equivalent function as the described core logic unit on page 5, lines 12-13 (Office Action p. 2.)

Applicants respectfully state that a term is entitled to its "plain meaning" definition in the art as well as all other associated definitions included within the present application.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea in View of U.S. Patent No. 5,909,559 to So.

Claims 1-5, 7, 10, 12 and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559).

Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 1-5, 7, 10, 12 and 20 are improper because the elements for a *prima facie* case of obviousness are not met. Specifically,

the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

Claim 1

Regarding amended independent claim 1, Applicants claim:

1. An apparatus for assisting in compressing video data in a computer system including a central processing unit and a system memory, comprising:
 - a video input port configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data;**
 - a video input buffer coupled to the video input port, for storing the video data from the video input port;**
 - a previous frame buffer, for storing at least a portion of a previous video frame;**
 - an operation unit coupled to the video input buffer and the previous frame buffer, for computing a difference frame from data from the video input buffer and data from the previous frame buffer; and**
 - a result buffer coupled to the operation unit and configured to couple with the system memory for temporarily buffering the difference frame prior to storing the difference frame in the system memory, the apparatus configured to operate within a north bridge chip of the computer system to enable the central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit.** (Emphasis added.)

Regarding claim 1, Dea and So do not appear to disclose an apparatus for assisting in compressing video data in a computer system including a central processing unit and a system memory, comprising: “a video input port configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data; a video input buffer coupled to the video input port . . . ; a previous frame buffer . . . ; an operation unit coupled to the video input buffer and the previous frame buffer . . . ; and a result buffer coupled to the operation unit and configured to couple with the system memory . . . ” as claimed by Applicants.

Specifically, Applicants’ apparatus for assisting in compressing video includes at least **two separate** interfaces, namely a video input port for coupling with the streaming video data from a video unit and a memory interface of the result buffer. Separate interfaces are not disclosed by Dea or So.

Specifically, Dea discloses and the Office Action concurs that the Dea architecture is bus oriented with the “apparatus” 120 of Dea being memory mapped to the bus with the bus being the only input and output from the “apparatus.” Specifically, Dea discloses that “[t]he information regarding the current frame line is received from bus interface 200”, (col. 6, lines 41-43) and “[w]hen accelerator 120 initiates actions it fetches thirty-two bit words from memory [and] [w]hen accelerator 120 is a target it responds to all scalar accesses or addresses in its range”, (col. 5, lines 2-5). Furthermore, according to the disclosure of Dea, “[t]ransmission . . . from . . . store buffer 248 to devices external to accelerator 120 is by way of accelerator bus interface 200.” (Col. 7, lines 42-44.) Such a bus architecture is further visibly supported by FIG. 2 of Dea.

Regarding the So reference, the Office Action cites So because it “discloses that a VSP (wrapper-and-digital signal processor-core) used as a graphic accelerator is provide either as the North bridge or AGP graphic/video chip as described at column 17, lines 24-43.” (See Office Action p. 5). Generally, So incorporates digital signal processors (DSPs) at one or more of the bridges, such as at the North bridge and/or South bridge so that the compression and decompression may occur inside of the DSPs of the bridges. So engages in additional compression/decompression complexity within the North bridge and does not disclose an apparatus for assisting in compressing video data in a computer system including a central processing unit and a system memory, comprising: “a video input port configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data; a video input buffer coupled to the video input port . . .; a previous frame buffer . . .; an operation unit coupled to the video input buffer and the previous frame buffer . . .; and a result buffer coupled to the operation unit and configured to couple with the system memory . . .” as claimed by Applicants. Therefore, Applicants respectfully request that the rejection to claim 1 be withdrawn.

Claims 2-5, 7, 10 and 12

Regarding claims 2-5, 7, 10 and 12, each of these claims includes additional elements that further distinguish from the cited references. In addition to claims 2-5, 7, 10 and 12 depending

either directly or indirectly from amended independent claim 1, each of these claims, as a whole, distinguish over the cited references. Therefore, Applicants respectfully request that the rejections to claims 2-5, 7, 10 and 12 be withdrawn.

Claim 20

Regarding amended independent claim 20, Applicants claim:

20. A computer system including resources for compressing video, comprising:
 - a central processing unit and system memory for further compressing the video within the computer system;
 - a video input port configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data;**
 - a video input buffer coupled to the video input port, for storing the video data from the video input port;
 - a previous frame buffer, for storing a least a portion of a previous video frame;
 - an operation unit coupled to the video input buffer and the previous frame buffer, for computing a difference frame from data from the video input buffer and data from the previous frame buffer; and
 - a result buffer coupled to the operation unit and configured to couple with the system memory for temporarily buffering the difference frame prior to storing the difference frame in the system memory, the video input port, the video input buffer, the previous frame buffer, the operation unit, and the result buffer configured to operate within a north bridge chip of the computer system to enable the central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit. (Emphasis added.)**

Regarding claim 20, Dea and So do not appear to disclose a computer system including resources for compressing video, comprising: “a central processing unit and system memory . . . ; a video input port configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data; a video input buffer coupled to the video input port . . . ; a previous frame buffer . . . ; an operation unit coupled to the video input buffer and the previous frame buffer . . . ; and a result buffer coupled to the operation unit and configured to couple with the system memory . . . ” as claimed by Applicants. Specifically, Applicants’ computer system including resources for compressing video includes at least **two separate**

interfaces, namely a video input port for coupling with the streaming video data from a video unit and a memory interface of the result buffer. Separate interfaces are not disclosed by Dea or So.

As previously stated, Dea's architecture is bus oriented with the resources for compressing video being memory mapped to the bus with the bus being the only input and output path. Applicants reiterate the above-arguments, namely, Dea discloses that “[t]he information regarding the current frame line is received from bus interface 200”, (col. 6, lines 41-43) and “[w]hen accelerator 120 initiates actions it fetches thirty-two bit words from memory [and] [w]hen accelerator 120 is a target it responds to all scalar accesses or addresses in its range”, (col. 5, lines 2-5). Furthermore, according to the disclosure of Dea, “[t]ransmission . . . from . . . store buffer 248 to devices external to accelerator 120 is by way of accelerator bus interface 200.” (Col. 7, lines 42-44.) Such a bus architecture is further visibly supported by FIG. 2 of Dea.

Regarding the So reference, Applicants sustain the previous arguments regarding the lack of disclosure of Applicants' claim elements with regard to claim 20. Therefore, Applicants respectfully request that the rejection to claim 20, be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea in View of U.S. Patent No. 5,909,559 to So and further in View of U.S. Patent No. 4,546,383 to Abramatic.

Claims 6 and 13-16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559) and further in view of Abramatic (U.S. Patent No. 4, 546, 383). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 6 and 13-16 are improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

Claim 6

Regarding claim 6, Dea, So, and Abramatic, either individually, or in any proper combination, do not teach, suggest, or motivate Applicants' invention of claim 6. Applicants sustain the arguments above that nothing within the four-corners of the cited references teach each and every element of Applicants' invention as claimed, including the elements of the base claim from which claim 6 depends. Namely, Dea, So, and Abramatic do not disclose an apparatus for assisting in compressing video data in a computer system including a central processing unit and a system memory, comprising: "a video input port configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data; a video input buffer coupled to the video input port . . .; a previous frame buffer . . .; an operation unit coupled to the video input buffer and the previous frame buffer . . .; and a result buffer coupled to the operation unit and configured to couple with the system memory . . ." as claimed by Applicants' claim 6. Therefore, Applicants respectfully request that the rejection to claim 6 be withdrawn.

Claims 13-16

Regarding claims 13-16, Dea, So, and Abramatic, either individually, or in any proper combination, do not teach, suggest, or motivate Applicants' invention of claims 13-16.

Regarding amended independent claim 13, Applicants claim:

13. An apparatus for compressing video data in a computer system including a central processing unit, comprising:

a video input port configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data;

a video input buffer coupled to the video input port, for storing the video data from the video input port;

a previous frame buffer, for storing a least a portion of a previous video frame; an exclusive-OR unit coupled to the video input buffer and the previous frame buffer, for computing a difference frame from data from the video input buffer and data from the previous frame buffer;

a result buffer coupled to the exclusive-OR unit for temporarily buffering the difference frame;

a **memory port** coupled to the previous frame buffer and the result buffer; and a **system memory coupled to the memory port** for storing the video data from the video input port and the difference frame from the result buffer, wherein the video data is stored to in a current frame in the memory, the apparatus configured to operate within a north bridge chip of the computer system to enable the central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit. (Emphasis added.)

Regarding claim 13, Dea, So and Abramatic do not appear to disclose an apparatus for assisting in compressing video data in a computer system including a central processing unit, comprising: “a video input port configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data; a video input buffer coupled to the video input port . . .; a previous frame buffer . . .; an exclusive-OR unit coupled to the video input buffer and the previous frame buffer . . .; and a result buffer coupled to the exclusive-OR unit . . .; a memory port coupled to the previous frame buffer and the result buffer; and a system memory coupled to the memory port . . .” as claimed by Applicants. Specifically, Applicants’ apparatus for assisting in compressing video includes at least a separate video input port for coupling with the streaming video data from a video unit and a memory port for coupling with the system memory. Separate interfaces are not disclosed by Dea, So or Abramatic.

As previously stated, Dea discloses and the Office Action concurs that the Dea architecture is bus-oriented with the “apparatus” 120 of Dea being memory mapped to the bus with the bus being the only input and output from the “apparatus.” Specifically, Dea discloses that “[t]he information regarding the current frame line is received from bus interface 200”, (col. 6, lines 41-43) and “[w]hen accelerator 120 initiates actions it fetches thirty-two bit words from memory [and] [w]hen accelerator 120 is a target it responds to all scalar accesses or addresses in its range”, (col. 5, lines 2-5). Furthermore, according to the disclosure of Dea, “[t]ransmission . . . from . . . store buffer 248 to devices external to accelerator 120 is by way of accelerator bus

interface 200.” (Col. 7, lines 42-44.) Such a bus architecture is further visibly supported by FIG. 2 of Dea.

The Office Action cites Dea and So for their alleged disclosure as previously herein rebutted. The Office Action continues by citing Abramatic for teaching “that XOR function for the difference calculation 56 which has the advantage of providing a less complicated means for the difference calculation techniques as elucidated at column 7, lines 32-35.” (See Office Action p. 14).

Applicants sustain the arguments above that nothing within the cited references teach each and every element of Applicants’ invention as claimed in amended independent claim 13. Specifically, Dea, So, and Abramatic do not teach, suggest, or motivate an apparatus for compressing video data in a computer system including a central processing unit, comprising: “a video input port configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data; a video input buffer coupled to the video input port . . .; a previous frame buffer . . .; an exclusive-OR unit coupled to the video input buffer and the previous frame buffer . . .; and a result buffer coupled to the exclusive-OR unit . . .; a memory port coupled to the previous frame buffer and the result buffer; and a system memory coupled to the memory port . . .” as claimed by Applicants’ amended independent claim 13. Therefore, Applicants respectfully request that the rejection to amended independent claim 13 be withdrawn.

Claims 14-16, 18 and 19

Regarding claims 14-16, 18 and 19, each of these claims includes additional elements that further distinguish from the cited references. In addition to claims 14-16, 18 and 19 depending either directly or indirectly from amended independent claim 13, each of these claims, as a whole, distinguish over the cited references. Therefore, Applicants respectfully request that the rejections to claims 14-16, 18 and 19 be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea in View of U.S. Patent No. 5,909,559 to So and Further in View of U.S. Patent No. 5,438,374 to Yan.

Claim 9 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559) and further in view of Yan (U.S. Patent No. 5, 438,374). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejection of claim 9 is improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

Regarding claim 9, Dea, So, and Yan, do not disclose an apparatus for assisting in compressing video data in a computer system including a central processing unit and a system memory, comprising: “a video input port configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data; a video input buffer coupled to the video input port . . . ; a previous frame buffer . . . ; an operation unit coupled to the video input buffer and the previous frame buffer . . . ; and a result buffer coupled to the operation unit and configured to couple with the system memory . . . ” as claimed by Applicants’ claim 9. Therefore, Applicants respectfully request that the rejection to claim 9 be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea in View of U.S. Patent No. 5,909,559 to So and Further in View of U.S. Patent No. 5,926,223 to Hardiman.

Claim 11 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559) and further in view of

Hardiman (U.S. Patent No. 5, 926, 223). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejection of claim 11 is improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

Regarding claim 11, Dea, So, and Hardiman, either individually, or in any proper combination, do not teach, suggest, or motive Applicants' invention as claimed in claim 11, including all of the claim limitations of the base claim, namely, do not disclose an apparatus for assisting in compressing video data in a computer system including a central processing unit and a system memory, comprising: "a video input port configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data; a video input buffer coupled to the video input port . . .; a previous frame buffer . . .; an operation unit coupled to the video input buffer and the previous frame buffer . . .; and a result buffer coupled to the operation unit and configured to couple with the system memory . . ." as claimed by Applicants' claim 11. Therefore, Applicants respectfully request that the rejection to claim 11 be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea in View of U.S. Patent No. 5,909,559 to So, in View of U.S. Patent No. 4,546,383 to Abramatic and further in view of U.S. Patent No. 5,438,374 to Yan.

Claim 18 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559) in view of Abramatic (U.S.

Patent No. 4,546,383) and further in view of Yan (U.S. Patent No. 5, 438, 374). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejection of claim 18 is improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

Regarding claim 18, Dea, So, Abramatic, and Yan, either individually, or in any proper combination, do not teach, suggest, or motive Applicants' invention as claimed, namely, Dea, So, Abramatic and Yen do not appear to disclose an apparatus for assisting in compressing video data in a computer system including a central processing unit, comprising: "a video input port configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data; a video input buffer coupled to the video input port . . .; a previous frame buffer . . .; an exclusive-OR unit coupled to the video input buffer and the previous frame buffer . . .; and a result buffer coupled to the exclusive-OR unit . . .; a memory port coupled to the previous frame buffer and the result buffer; and a system memory coupled to the memory port . . ." as claimed by Applicants. Specifically, Applicants' apparatus for assisting in compressing video includes at least a separate video input port for coupling with the streaming video data from a video unit and a memory port for coupling with the system memory. In support, Applicants sustain the arguments above as applied to the base claim. Therefore, since Dea, So, Abramatic or Yan, either individually or in any proper combination, do not teach, suggest, or motivate Applicants' invention as claimed in claim 18, Applicants respectfully request that the rejection to claim 18 be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea in View of U.S. Patent No. 5,909,559 to So, in View of U.S. Patent No. 4,546,383 to Abramatic and further in view of U.S. Patent No. 5,926,223 to Hardiman.

Claim 19 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559) in view of Abramatic (U.S. Patent No. 4,546,383) and further in view of Hardiman (U.S. Patent No. 5,926,223). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejection of claim 19 is improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

Regarding claim 19, Dea, So, Abramatic, and Hardiman, either individually, or in any proper combination, do not teach, suggest, or motive Applicants' invention as claimed, namely, Dea, So, Abramatic and Hardiman do not appear to disclose an apparatus for assisting in compressing video data in a computer system including a central processing unit, comprising: "a video input port configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data; a video input buffer coupled to the video input port . . .; a previous frame buffer . . .; an exclusive-OR unit coupled to the video input buffer and the previous frame buffer . . .; and a result buffer coupled to the exclusive-OR unit . . .; a memory port coupled to the previous frame buffer and the result buffer; and a system memory coupled to the memory port . . ." as claimed by Applicants. Specifically, Applicants' apparatus for assisting

in compressing video includes at least a separate video input port for coupling with the streaming video data from a video unit and a memory port for coupling with the system memory.

Therefore, since Dea, So, Abramatic or Hardiman, either individually or in any proper combination, do not teach, suggest, or motivate Applicants' invention as claimed in amended claim 19. Applicants respectfully request that the rejection to claim 19 be withdrawn.

Applicant submits that claims 1 through 7, 9 through 16 and 18 through 20 are clearly allowable over the cited prior art.

Applicant requests the allowance of claims 1 through 7, 9 through 16 and 18 through 20 and the case passed for issue.

Respectfully submitted,



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